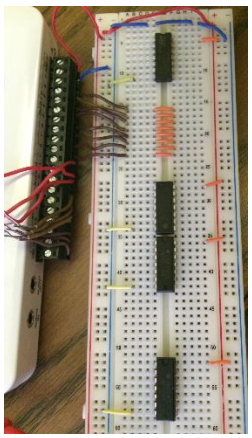
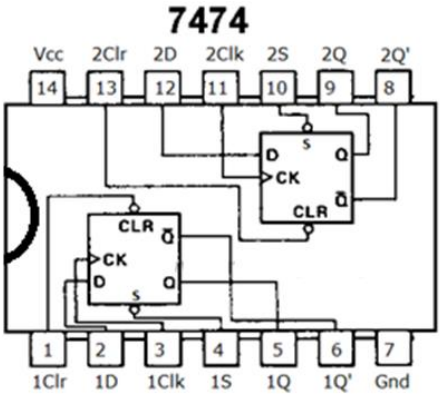
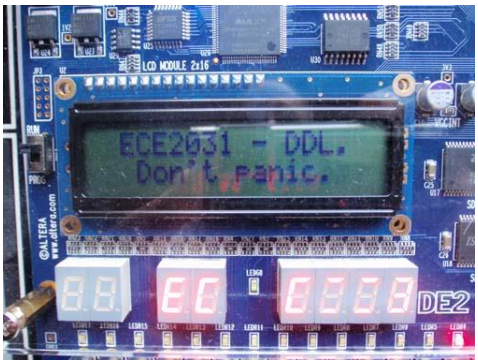
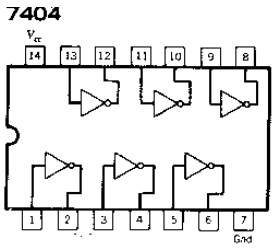
DIGITAL CIRCUIT DEBUGGING GUIDE FOR ECE 2020 & ECE 2031

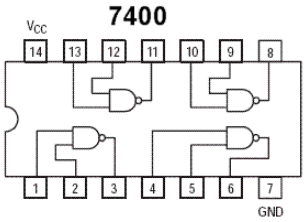
For ECE 2020 and ECE 2031

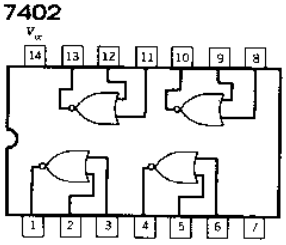












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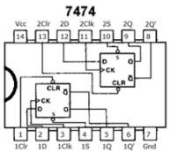
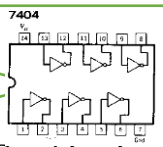
Don't panic. You do not need to read the whole document. Just follow the flowchart. Skip to where you know where the problem lies.

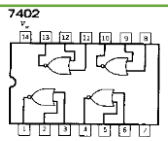
This guide is to help students taking ECE2020 and ECE2031 debug their digital circuits systematically. This document is not meant to find problems in k-maps or logic diagrams.

When probing, the correct reading should be predicted before being tested, and then compared with tested value.



Is the circuit sequential or combinational logic?





Sequential (D-Flip flops)

Combinational (not, nand, nor)

Make sure the clock and reset are set up correctly. *,**, ****

Pg. 7

ECE2031: Pushbutton setup.....
Pg. 31 Figure 2.14 of lab manual

Reset all states. Sequentially go through all state transitions, until problem is found.

Incorrect State transition

Reset and go back to state right before incorrect output. Check flip-flop's pins, starting with input D.

Pg. 8

Retry

Is input D incorrect?

D incorrect

Go through all the input combinations, seeing which combination give incorrect outputs. *,**

Are there many problems or a few?

Few

Work backwards. Start probing from the last output.

Pg. 6.2

Many

Work forwards. Start probing from the first input.

Pg. 6.1

If all pins leading to gate are correct, but output is still wrong, something is wrong with chip, breadboard or its connection to the breadboard.

Pg. 5 - Nothing seems wrong!!!

Good Habits and common mistakes

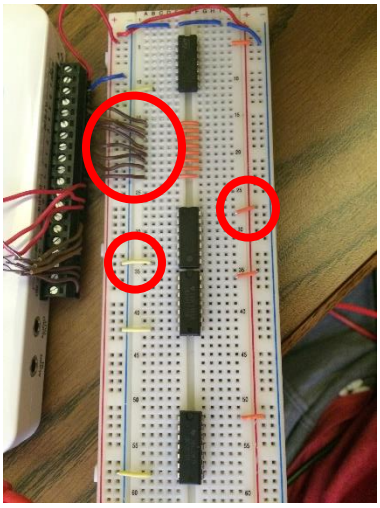


Figure 1. Default setup of breadboard.

Set up the 5V and the ground of each pin with small wires before starting anything else. Color code the rest. For example, not gate outputs could be red, and Nand gate outputs could be blue.

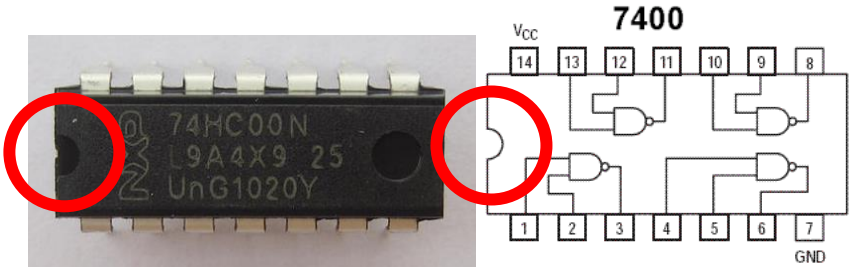


Figure 2. The left-side of the semicircle is pin 1.[1]

Make sure the pin is not upside down. Make sure you are using the correct chip.

7404 – Not Gate

7400 – Nand / Bor

7402 - Nor

7474 – D-Flip Flop

Debugging by probing: Whenever something does not work, it is a good idea to see if whatever is being used to observe the output can also be used to probe an intermediate part of the system in order to help break down the problem. Here, the myDaq or DE2 board can be used probe the middle of the circuit, even though their main function is to measure the output.

[1] Singh, Shantnu. "Basic ICs." *Unbolting Binary*. N.p., n.d. Web. 11 July 2016

Probing for ECE 2020

A probe is the main tool for debugging. It is done so that *any* part of the circuit can be checked, *not* just the final output. The myDAQ allows the user to check whether a wire is a digital 1 or 0, by reading the voltage of a node.

Method 1: NI Elvis Digital Reader

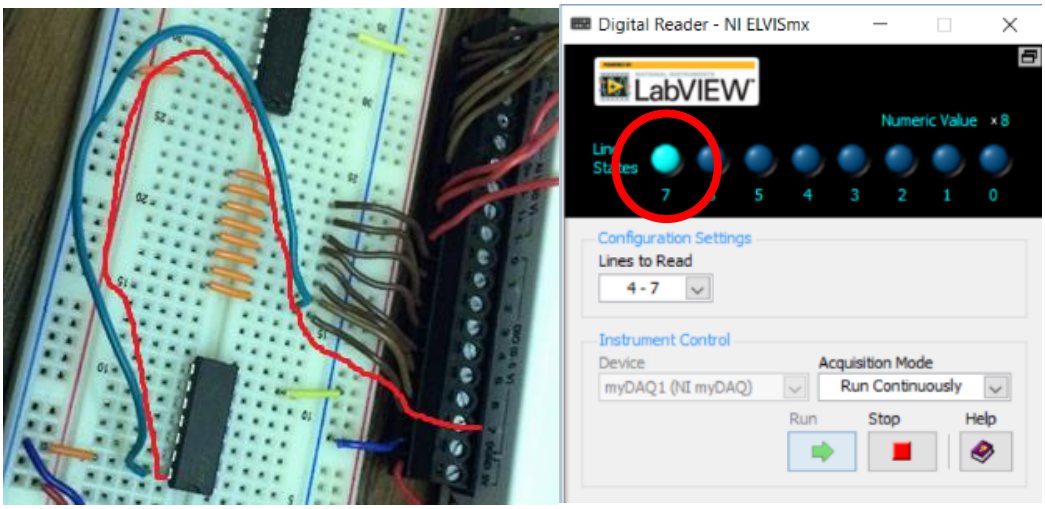


Figure 3. A wire connected to DIO7 is probing pin 14 (Vcc) of the chip which is confirmed to be a digital 1 using the NI ELVIS Digital Reader.

In the lab assignments, the NI ELVIS Digital Reader is used to read the circuit outputs. But the same wire that is used to probe any part of the circuit. In *Figure 3*, a DIO7 of myDaq is used to check if the Vcc of the chip is in fact a digital 1.

Method 2: NI Elvis Digital Multimeter

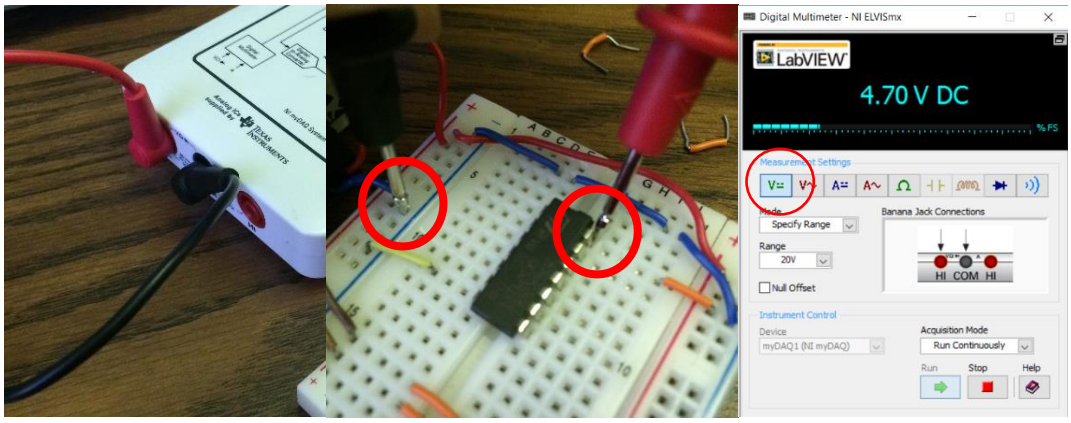


Figure 4. The NI ELVIS Digital Multimeter can be used to probe digital circuits.

The NI ELVIS Digital multimeter when set to 20V range can probe a circuit. The negative black terminal is touching any digital ground (DGND) and the positive red to probe any part of the circuit

Probing for ECE 2031

A probe is the main tool for debugging. It is done so that *any* part of the circuit can be checked, *not* just the final output. The DE2 board allows the user to check whether a wire is a digital 1 or 0, by reading the voltage of a node.

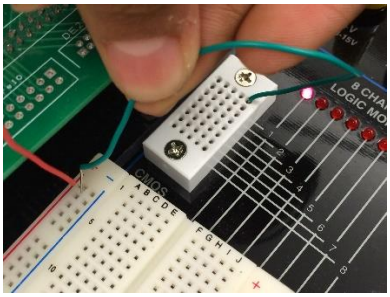


Figure 5. A wire connected to the 8 channel logic monitor, is being used to confirm that the VCC terminal is a digital 1.

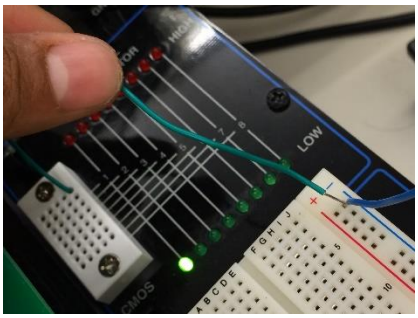


Figure 6. A wire connected to the 8 channel logic monitor is being used to confirm that the Ground terminal of the breadboard is a digital 0.

The device being used to read the final output (the 8 channel logic monitor) is also used to probe the circuit. In *Figure 5*, whenever there is a digital 1, the corresponding light is red and green when there is a digital 0, shown in *Figure 6*. Note that the logic monitor should also be set to TTL, shown in *Figure 7*.

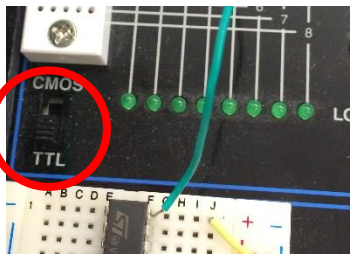


Figure 7. The Logic Monitor should be set to TTL, not CMOS.

Problems that appear when probing the pins

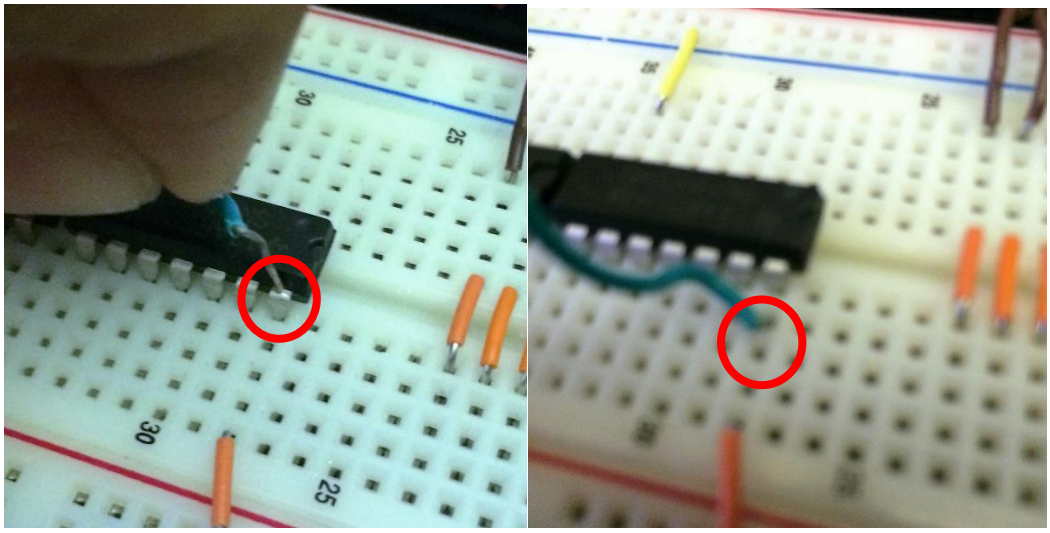
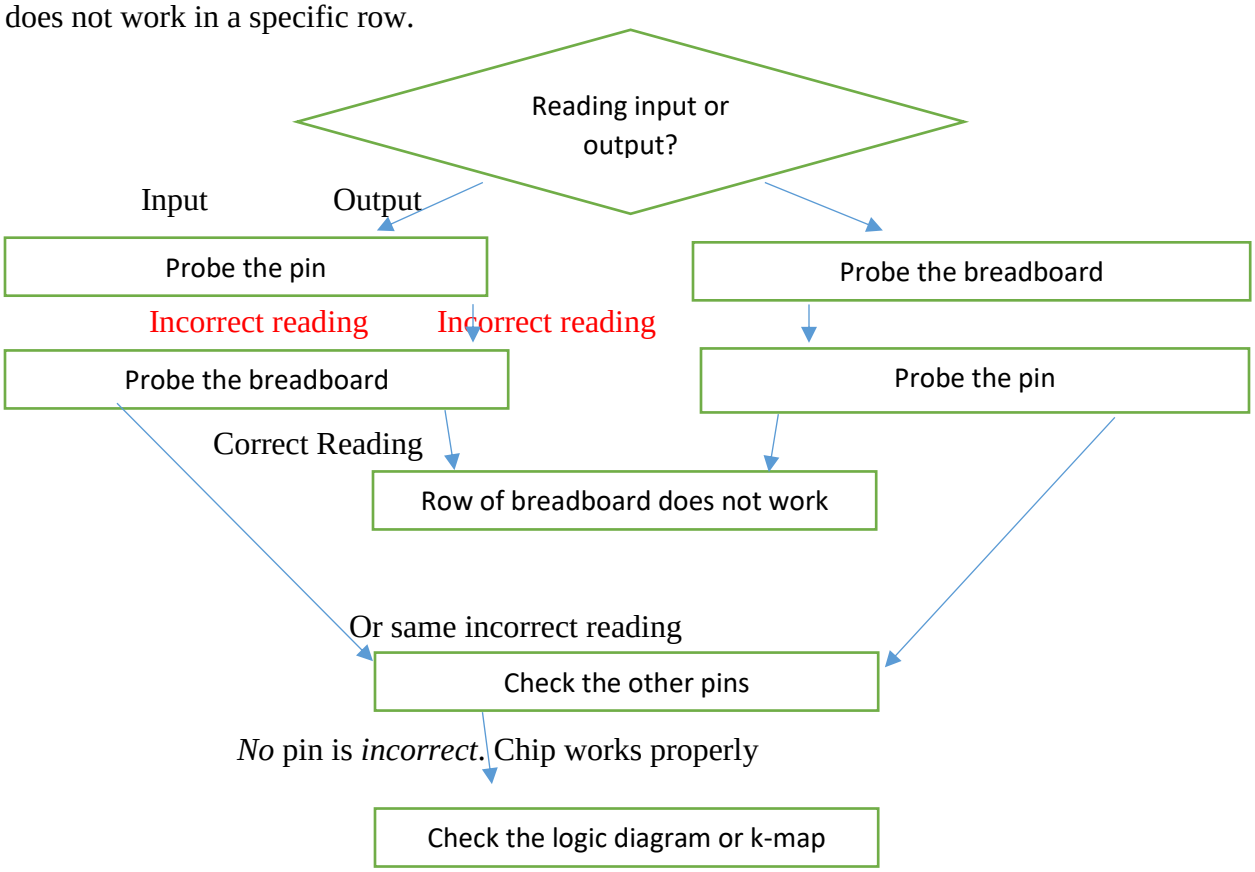


Figure 8. The green wire is used as a probe can either check the pin directly (shown left), or the node directly connected to the pin (shown right).

When probing the input of a chip, touch the pin directly with the wire. When probing the output, insert the pin into the breadboard. This is done in the small possibility that the breadboard does not work in a specific row.



Debugging Combinational Problems

Many Problems

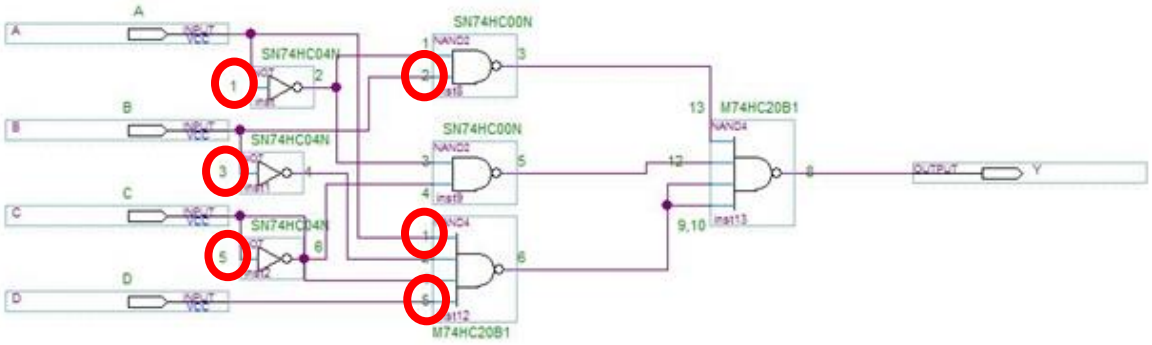


Figure 9. Pins 1, 3, and 5 of a not gate, and pins 3 and 5 of nand gate are highlighted.

If there are many incorrect outputs of Y, after trying every input combination, then check the pins of the inputs of the gates closest to the circuit input. In *Figure 9*, the inputs of the not chip and the nand chip are probed. For example, pin 1 of not gate should be 1 when A is, so probe it to confirm this is the case.

Few Problems

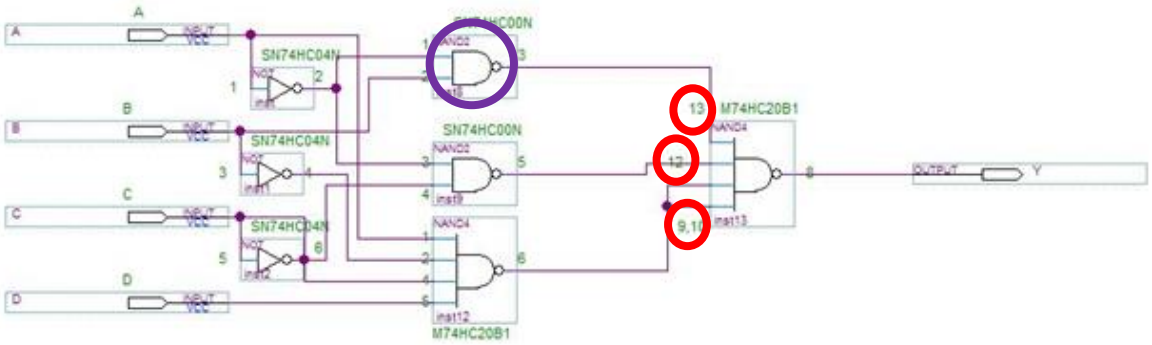


Figure 10. Pins 9, 10, 12, and 13 of the last gate are highlighted.

If there are few incorrect outputs of Y, after trying every input combination, then check the pins of the inputs of the gates closest to the circuit output. In *Figure 10*, the inputs of the last chip are probed. In this example, the value of pin 13 is probed, whilst every input combination that affects it (A and B in this case) is tested. If pin 13 is correct, repeat for pins 12 and 9 and 10.

D incorrect: *Red circle 13 on Figure 10.*

If pin 13 (or D) is incorrect, then check the inputs of the gate that creates its values (the gate circled purple).

If no error is yet found, refer to Pg. 5.

Checking the clock and reset

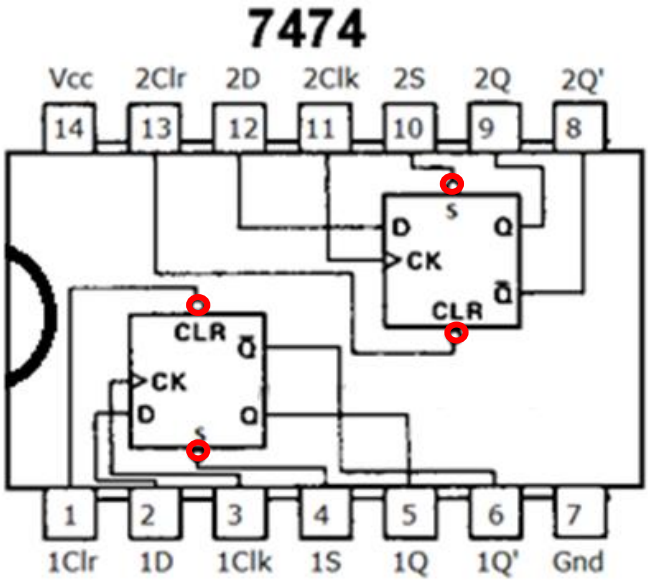


Figure 11. Pin configuration of a D flip-flop.[2]

* Confirm that the chip is in fact a D flip-flop, and that it is facing the correct direction. The orientation is discerned by the semi-circle cutaway on one of its sides.

**** *Attention:* The set (PRESET) and reset (CLR) are active low, shown by the bubbles on the logic gates, painted red here in *Figure 11*. This means that rather than the output Q being 0 when CLR is 1, Q is 0 when CLR is 1. Similarly, rather than the output Q being 1 when Set is 1, Q is 1 when Set is 0. The input condition is merely inverted, which can be denoted as $\overline{Preset}$ and $\overline{Clear}$.

Therefore, $\overline{Preset}$ and $\overline{Clear}$ should never be connected to a 0, and in the assigned labs, $\overline{Preset}$ should always be 1.

** Next confirm that Vcc is 1, and Gnd is 0.

Now, rather than probing the output, prove the input to confirm that when the clock is correctly connected to its intended input, and that it changes value correctly.

Finally check the value of D and press the clock. The Q value should become the previous Q value. If this does not work as intended, go to Pg. 5.

[2] Vp, Jaseem. "Johnson Digital Counter Circuit Diagram Using D Flip Flop 7474 (3 Bit/4 Bit) with Animation/ Simulation - *Circuits Gallery*." Circuits Gallery. N.p., 02 July 2012. Web. 11

Correcting Incorrect State Transition

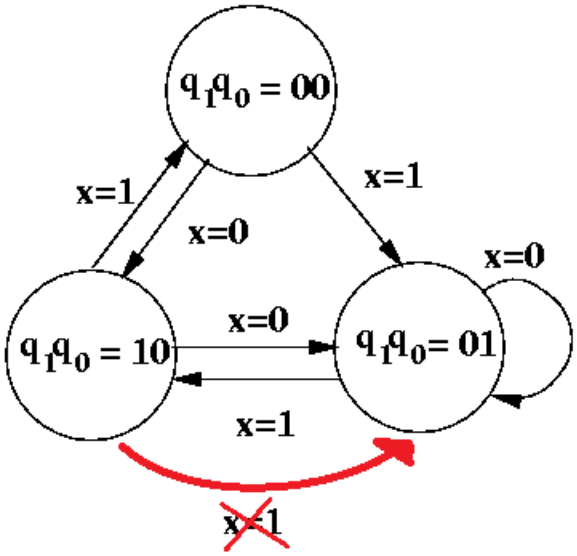


Figure 12. Example Moore state machine, were when X = 0, State 10 goes to 01, when it should go to 00.[3]

When there is an incorrect state transition, the D input of the D flip-flop that made the next state incorrect should be checked. In *Figure 12*, when x = 1, it transitions from state 10 to 01 when it should go to 11. This means that q0 is incorrect, because it becomes 1 when it should become 0. To find the exact problem, the state machine should be reset, and brought back to state 10. Then, when x = 0, rather than switching to the next state, the value of the input of the q0 flip-flop should be checked, and it is supposed to be incorrect. If this is the case, go to Pg. 5.2: **D incorrect** to fix the D input.

[3] "Finite State Machines with Output (Mealy and Moore Machines)." *Finite State Machines with Output (Mealy and Moore Machines)*. N.p., n.d. Web. 11 July 2016.

Reference

Collins, Thomas. *Digital Design*. S.l.: Kendall Hunt, 2009. 31. Print.

[3] "Finite State Machines with Output (Mealy and Moore Machines)." *Finite State Machines with Output (Mealy and Moore Machines)*. N.p., n.d. Web. 11 July 2016. https://www.cs.umd.edu/class/sum2003/cmsc311/Notes/Seq/fsm.html

[1] Singh, Shantnu. "Basic ICs." Unbolting Binary. N.p., n.d. Web. 11 July 2016. http://unboltingbinary.in/electronics-and-robotics/basic-ics-and-their-pin-diagram/

[2] Vp, Jaseem. "Johnson Digital Counter Circuit Diagram Using D Flip Flop 7474 (3 Bit/4 Bit) with Animation/ Simulation - Circuits Gallery." *Circuits Gallery*. N.p., 02 July 2012. Web. 11 http://www.circuitsgallery.com/2012/07/johnson-digital-counter-circuit-diagram.html